Examination Nov/Dec 2019

H-434

Total No. of Printed Pages:3

SUBJECT CODE NO:- H-434
FACULTY OF SCIENCE AND TECHNOLOGY
S.E. (EEE) (Sem-I)
Electronics Devices and Circuit
[OLD]

[Time: Three Hours]   **[Max. Marks:80]**

Please check whether you have got the right question paper.

N.B.: i) Question No.1 & 6 are compulsory.

ii) Solve any two questions from each section from the remaining questions.

iii) Assume suitable data if necessary

Section – A

Q.1   Answer following questions (Any five)   10
   a) What is Ripple factor?
   b) What is Load regulation?
   c) What is early effect in transistor?
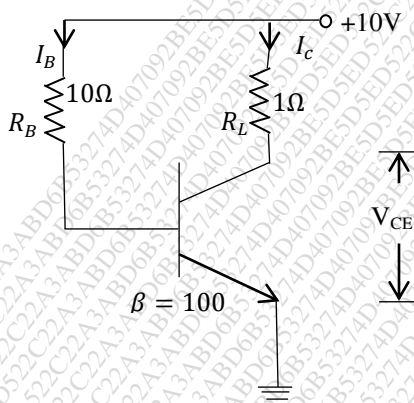   d) Find out whether the transistor of fig "a" is working in saturation or well into saturation.

Fig "a"

   e) Draw the equivalent circuit of FET & Transistor.
   f) Draw FET self biasing circuit. State advantages.
   g) What is the necessity of transistor stabilization?
   h) A FET has a driven current of 4mA. If $I_{DSS} = 8mA$ and $V_{GS}(off) = -6V$. Find the value of V_{GS} and V_P.

Q.2   (A) Explain the operation of full wave rectifier.   08
        A full wave rectifier supplies a Load of 1KΩ. The a.c. voltage applied to the diode is
        200-0-200 Vrms. If diode resistance is neglected, calculate,
        (i)   Average dc voltage.
        (ii)   Average dc current
        (iii)   Ripple voltage (rms)

       (B) Draw and explain the operation of voltage multiplier circuit using diode. State   07
       applications.

Q.3   (A) Compare between JFET and MOSFET.   08
       (B) Explain how a transistor can be tested by different methods.   07

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Q.4   (A) For the voltage divider bias configuration of fig "b", Determine (i) I_C (ii) V_E (iii) V_{CC} 08
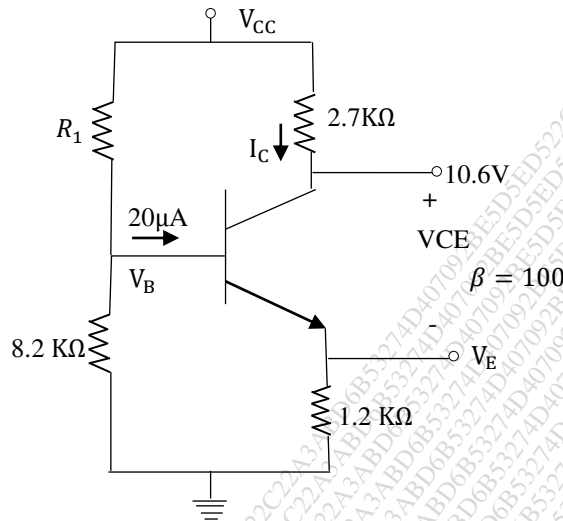(iv) V_{CE} (v) V_B and (vi) R_1

Fig "b"

(B) Draw and explain fixed bias method for transistor. Calculate stability factor for fixed   07
base biasing without emitter resistor.

Q.5   Write notes on,   15
(a) Transistor as a SWITCH
(b) LC Filter
(c) Power MOSFET

Section – B

Q.6   Answer the following (Any five)   10

a) What are the advantages of Negative feedback?
b) What is Cascade amplifier?
c) What are hybrid parameters?
d) Draw emitter follower circuit.
e) State Miller's theorem.
f) What is Push pull amplifier?
g) In a transistorized Hartley oscillator, the tank circuit has the capacitance of 100pF.
The value of inductance between the collector and tapping point is 30mH and the
value of inductance between the tapping point and the transistor base is $1 \times 10^{-8} H$.
Determine the frequency of oscillations. Neglect the mutual inductance.
h) Draw single tuned amplifier.

Q.7   (A) Draw and explain the operation of Transformer coupled amplifier. State its   08
advantages and comment on frequency response of transformer coupled amplifier.
(B) What is Differential amplifier? Explain.   07

Q.8   (A) For the circuit shown in fig (c), the transistor used has the following h-parameters: 08
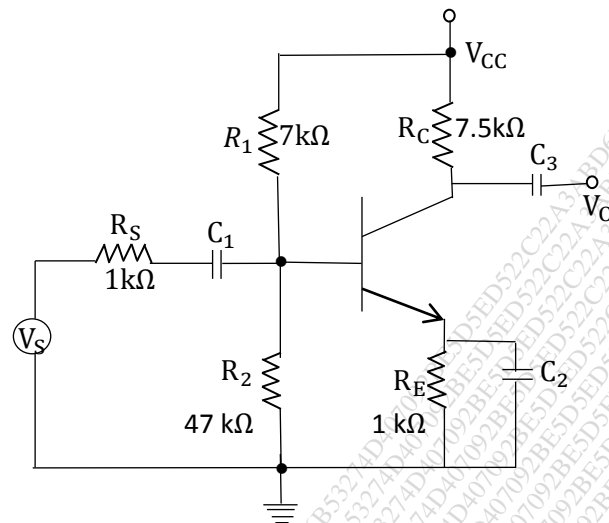$h_{ie}=1.1K\Omega$, $h_{oe}=2.5 \times 10^{-4}$, $h_{fe}=50$, $h_{re}=25$ μA/V.

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Fig "c"

Determine A_{is}, A_{vs}, R_i and R_o assuming all capacitors to be arbitrarily large.

(B) Explain the operation of complementary symmetry push pull amplifiers. 07

Q.9 (A) With neat circuit diagram explain working of CRYSTAL oscillator. State advantages. 08

(B) Explain the effect of Junction capacitance in high frequency amplifiers. 07

Q.10 Write note on, 15
   a) Stager tuned amplifier
   b) Wide Band amplifier
   c) Class C power amplifier.