Total No. of Printed Pages:02

SUBJECT CODE NO:- H-374
FACULTY OF SCIENCE AND TECHNOLOGY
B.E. (EC/ECT/E&C) (Sem-I)
VLSI Design
[OLD]

[Time: Three Hours] **[Max. Marks:80]**

Please check whether you have got the right question paper.

N.B.: 1) Question No. 1 & Question No. 6 are compulsory.
2) Solve any two question from Q. no. 2 to Q. No.5
3) Solve any two question from Q. No. 7 to Q. No. 10
4) Figure to the right indicates full marks.
5) Assume suitable data if necessary.

Section - A

Q.1 Attempt any two from the following: 10

a) What are basic elements of VHDL?
b) Compare with function and procedure in VHDL.
c) Write Syntax for signal, variable and constant in VHDL.
d) Define the term controllability and observability.

Q.2 a) Explain the operator used in VHDL. 07
b) Compare different types of modeling in VHDL. 08

Q.3 a) Draw and explain architecture of XC4000 FPGA family. 07
b) Write VHDL Code for D Flip Flop with its test bench. 08

Q.4 a) What is test bench? Write a test bench to verify design of NOR gate. 07
b) Write a VHDL code to design 8:1 Multiplexer with test bench. 08

Q.5 Write short notes on any three 15

i) Architecture of XC9500 FPGA
ii) Package and Library
iii) BIST
iv) TAP Controller

Section B

Q.6 Attempt any two from the following:- 10

a) What is Velocity Saturation in CMOS?
b) What is Noise Margin & Power delay Product?
c) Explain Junction Leakage and Tunnelling Effect in CMOS.

d) What is Pass Transistor explain in details.

Q.7 a) What are types of CMOS Logic families and define ratios circuit. 07

b) Explain with the help of neat diagram operation of CMOS inverter & its I-V characteristics. 08

Q.8 a) Draw the 4:1 multiplexer using transmission gates. 07

b) Sketch schematic for the following equation using CMOS $Y = AB + \bar{C}\bar{D}$ 08

Q.9 a) Draw layout of CMOS inverter circuit and explain the layout DRC. 07

b) Sketch schematic for the following equation using CMOS $Y = ABC + \bar{E}\bar{F}\bar{G}$ 08

Q.10 Write short notes on (any three) 15

a) Body Effect in CMOS
b) Power Dissipation in CMOS
c) Stick Diagram
d) Transmission Gates