Total No. of Printed Pages:2

SUBJECT CODE NO:- H-1082
FACULTY OF SCIENCE AND TECHNOLOGY
S .Y B.Tech. (CSE) CBC & Grading System (Sem IV)
Computer Organization
[Revised]

[Time: Three Hours] **[Max.Marks: 80]**

Please check whether you have got the right question paper.

N.B
1) Q.No.1 and Q.No.6 are compulsory.
2) Attempt any two questions from remaining questions from each section.

Section A

Q.1 Attempt any five: 10
a) Define: Computer Architecture.
b) Subtract -2 & -6 using 2's complement subtraction.
c) Draw the flowchart of Booth's algorithm.
d) Draw the diagram of Micro programmed control unit.
e) CISC is ……
f) Enlist the Processor elements.
g) Draw the CPU with internal BUS architecture.

Q.2 a) Write short note on 2's complement addition &subtraction. 08
b) Explain Pentium processor. 07

Q.3 a) Write short note on processor organization. 08
b) Explain Booth's algorithm. 07

Q.4 a) Perform Multiplication of -2 (Multiplicand) and 3 (Multiplier) using Booth's. 08
b) Write a note on Instruction cycle. 07

Q.5 a) Explain Hardwired Control unit. 08
b) Write a note on RISC. 07

Section B

Q.6 Attempt any five: 10
a) What is Cache miss?
b) Enlist advanced processors.
c) Draw 4 stage pipelining mechanism
d) Define: MMU
e) Enlist Pipeline hazards
f) Why virtual memory is required?
g) Draw Memory Hierarchy.

Q.7	a)	Write a note on Dual core processor.	08
	b)	Describe Virtual memory.	07
Q.8	a)	Explain Cache memory mapping techniques.	08
	b)	Explain memory hierarchy.	07
Q.9	a)	Describe data hazard with suitable example.	08
	b)	Write advantaged & disadvantages of pipelining.	07
Q.10	a)	Write a short note on Cache memory.	08
	b)	Explain performance of pipelining.	07